Notice of Allowability	Application No.	Applicant(s)	
	09/757,404	GUCCIONE ET AL.	
	Examiner	Art Unit	
	Mary C Hogan	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Response to Final Office Action dated 2/9/05*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ The drawings filed on *8/20/04* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

DETAILED ACTION

AND

REASONS FOR ALLOWANCE

1. This communication is in response to Applicants' Response to Final Office Action, dated 2/9/05.

Withdrawal of Rejections Under Section 103

2. Applicants' arguments are sufficient to remove the rejections under 35 USC 103 (a).

Reasons for Allowance

3. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) constructing objects corresponding to a series of logic gates and signals, each object having associated therewith an output signal state and one or more input signal states, scheduling events for signals to change states according to a stimulus specification, for each event, updating the output signal state and an input signal state of a corresponding object in response to the input signal state of the event, and finding elements connected to the output signal (U.S. Patent Number 6,466,898);

(2) FPGA's are a subclass of PLD's, configurable logic blocks that contain look up tables (LUTs), configuration code, timing constructs defining whether signals are synchronous or asynchronous, propagation delay, simulating a placed logic design to determine how the implemented FPGA design will perform (U.S. Patent Number 6,216,257);

(3) event driven simulation, emulation, event queues for simulation of an FPGA design (Bauer et al, "A Reconfigurable Logic Machine for Fast Event-Driven Simulation", Design Automation Conference Proceedings (DAC), June, 1998, pages 668-671).

3.1 Applicants' claims consist of claims 1-19 and 20.

Independent claim 1 is directed to a method for simulating a circuit design for a programmable logic device (PLD); independent claim 20 is the corresponding apparatus claim. Each independent claim identifies the distinct limitations of "generating events in response to signal values in the configuration bitstream, each event including an object identifier, an input signal identifier and an input signal state".

Because the closest prior art does not appear to teach or suggest that the events are generated in response to signal values in the configuration bitstream, and wherein the event includes an input signal identifier, Claims 1-20 are deemed allowable.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record, see PTO 892, and not relied upon is considered pertinent to applicant's disclosure, careful consideration must be given prior to Applicant's response to this Office Action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C Hogan whose telephone number is 571-272-3712. The examiner can normally be reached on 7:30AM-5PM Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary C. Hogan
Assistant Patent Examiner
Art Unit 2123

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